Claims

What is claimed is:

1. A method used during the formation of a semiconductor device, comprising:

forming a polysilicon layer;

forming a titanium nitride layer on the polysilicon layer;

forming a tungsten nitride layer on the titanium nitride layer;

forming an amorphous conductive layer on the tungsten nitride layer; and

forming a tungsten metal layer on the amorphous conductive layer.

2. The method of claim 1 further comprising:

etching each of the polysilicon layer, the titanium nitride layer, the tungsten nitride layer, the amorphous conductive layer, and the tungsten metal layer to define a transistor gate stack.

3. The method of claim 1 further comprising:

removing a portion of the polysilicon layer to define a conductive digit line contact plug;

etching each of the titanium nitride layer, the tungsten nitride layer, the amorphous conductive layer, and the tungsten metal layer to define a digit line.

4. The method of claim 1 further comprising forming an amorphous refractory metal silicide layer during the formation of the amorphous conductive layer.

5. The method of claim 1 further comprising forming an amorphous tantalum silicide layer during the formation of the amorphous conductive layer.

6. The method of claim 1 further comprising forming an amorphous tungsten silicide layer during the formation of the amorphous conductive layer.

7. A method used to form a semiconductor device, comprising:

forming a polysilicon layer;

forming a conductive barrier layer on the polysilicon layer;

forming a conductive nitride layer on the conductive barrier layer, wherein the conductive nitride layer forms on the conductive barrier layer as a crystalline layer;

forming a conductive amorphous layer on the conductive nitride layer; and

forming an elemental metal layer on the conductive amorphous layer, wherein the elemental metal layer forms on the conductive amorphous layer as an amorphous layer.

8. The method of claim 7 further comprising:

etching each of the polysilicon layer, the conductive barrier layer, the conductive nitride layer, the conductive amorphous layer, and the elemental metal layer to define a transistor gate stack.

9. The method of claim 7 further comprising:

removing a portion of the polysilicon layer to define a conductive digit line contact plug; and

etching each of the conductive barrier layer, the conductive nitride layer, the conductive amorphous layer, and the elemental metal layer to define a digit line.

10. The method of claim 7 further comprising forming an amorphous refractory metal silicide during the formation of the conductive amorphous layer.

11. The method of claim 7 further comprising forming a tantalum silicide layer during the formation of the conductive amorphous layer.

12. The method of claim 7 further comprising forming an amorphous tungsten silicide layer during the formation of the conductive amorphous layer.

13. A transistor gate for a semiconductor device, comprising:

a polysilicon layer;

a titanium nitride layer contacting the polysilicon layer;

a tungsten nitride layer contacting the titanium nitride layer;

an amorphous conductive layer contacting the titanium nitride layer; and

tungsten metal layer contacting the amorphous conductive layer.

14. The transistor gate of claim 13 wherein said amorphous conductive layer is an amorphous refractory metal silicide layer.

15. The transistor gate of claim 13 wherein said amorphous conductive layer is an amorphous tantalum silicide layer.

16. The transistor gate of claim 13 wherein said amorphous conductive layer is an amorphous tungsten silicide layer.

17. The transistor gate of claim 13 wherein said transistor gate is part of a word line for a semiconductor memory device.

18. A digit line and digit line plug for a semiconductor device, comprising:

a polysilicon layer;

a titanium nitride layer contacting the polysilicon layer;

a tungsten nitride layer contacting the titanium nitride layer;

an amorphous conductive layer contacting the titanium nitride layer; and

tungsten metal layer contacting the amorphous conductive layer.

19. The conductive plug of claim 18 wherein said amorphous conductive layer is an amorphous refractory metal silicide layer.

20. The conductive plug of claim 18 wherein said amorphous conductive layer is an amorphous tantalum silicide layer.

21. The conductive plug of claim 18 wherein said amorphous conductive layer is an amorphous tungsten silicide layer.